UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/716,600	11/20/2003	Colin Wilson	040849-0254	7174

41838 7590 07/28/2004

GENERAL ELECTRIC COMPANY (PCPI)
C/O FLETCHER YODER
P. O. BOX 692289
HOUSTON, TX 77269-2289

EXAMINER	
WILLIAMS, JOSEPH L	

ART UNIT	PAPER NUMBER
2879	

DATE MAILED: 07/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

A

Office Action Summary	Application No.	Applicant(s)	
	10/716,600	WILSON, COLIN	
	Examiner	Art Unit	
	Joseph L. Williams	2879	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19-37,42 and 43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19-37,42 and 43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/20/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: There is no mention of the parent application (for example: "This application is a divisional of 10/235,555 filed 09/06/2002, now US 6,670,629").

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 19, 24, 27, 42, and 43 are rejected under 35 U.S.C. 102(b) as being anticipated by Jaskie et al. (US 5,606,215).

Regarding claim 19, Jaskie ('215) teaches in the figure and in column 1, line 42 through column 2, line 64, a method of forming a field emitter device (10) on a substrate (11), the method comprising: forming a first insulating layer (12) on the substrate; forming a conducting gate layer (17) having a top surface and at least one side surface on the first insulating layer; forming a field emitter tip (14) on the substrate adjacent the first insulating layer and the conducting layer; and forming a second insulating layer (19) on at least one side surface of the conducting gate layer adjacent the field emitter tip to prevent arcing between the field emitter tip and the conducting gate layer.

Regarding claim 24, Jaskie ('215) teaches that forming a second insulating layer comprises: selectively depositing a second insulating material on the conducting gate layer.

Regarding claim 27, Jaskie ('215) teaches the forming a second insulating layer further comprises: forming the second insulating material over the top surface of the conducting gate layer.

Regarding claim 42, Jaskie ('215) teaches, similar to claim 19 above, a method of forming a field emitter device on a substrate, the method comprising: forming a first insulating layer on the substrate; forming a conducting gate layer having a top surface and at least one side surface on the first insulating layer; forming a field emitter tip on the substrate adjacent the first insulating layer and the conducting layer; and forming an arc prevention layer on at least one side surface of the conducting gate layer adjacent the field emitter tip to prevent arcing between the field emitter tip and the conducting gate layer.

Regarding claim 43, Jaskie ('215) teaches that the arc prevention layer is a dielectric material.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 20, 22, 23, 25, 26, 28-32, 34, and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jaskie et al. (US 5,606,215), of record, in view of Tjaden et al. (US 6,190,223).

Regarding claim 20, Jaskie ('215) teaches all of the claimed limitations except for the first insulating layer being formed by blanket depositing a first insulating material over the substrate; and patterning the first insulating material.

Further regarding claim 20, Tjaden ('223) teaches in the abstract and in figures 4-10, a method of forming a field emitter device comprised of, in part, forming the first insulating layer being formed by blanket depositing a first insulating material over the substrate; and patterning the first insulating material for the purpose of saving time and cost during the manufacturing process.

Hence it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the manufacturing steps of Tjaden on the field emission device of Jaskie for the purpose of saving time and cost during the manufacturing process.

Regarding claim 22, Tjaden ('223) teaches the first insulating material comprises one silicon oxide, silicon nitride, and silicon oxynitride.

The reason for combining is the same as for claim 20 above.

Regarding claim 23, Tjaden ('223) teaches the forming a second insulating layer comprises: blanket depositing a second insulating material over the conducting gate layer; and patterning the second insulating material.

The reason for combining is the same as for claim 20 above.

Regarding claim 25, Tjaden ('223) teaches forming a second selectively depositing a second insulating material on the gate conducting layer and the first insulating layer.

The reason for combining is the same as for claim 20 above.

Regarding claim 26, Tjaden ('223) teaches forming a second insulating layer comprises: depositing a second insulating material on the gale conducting layer using the first insulating layer and the conducting gate layer as a shadow mask.

The reason for combining is the same as for claim 20 above.

Regarding claim 28, Tjaden ('223) teaches the second insulating material comprises one silicon oxide, silicon nitride, and silicon oxynitride.

The reason for combining is the same as for claim 20 above.

Regarding claim 29, Tjaden ('223) teaches the forming the conducting gate layer comprises: depositing a conducting material on the first insulating layer; and patterning the conducting material to form the conducting gate layer.

The reason for combining is the same as for claim 20 above.

Regarding claim 30, Jaskie ('215) teaches the conducting material comprises a refractory metal.

Regarding claim 31, Tjaden ('223) teaches depositing a conducting material on the substrate; and patterning the conducting material.

The reason for combining is the same as for claim 20 above.

Regarding claim 32, Jaskie ('215) teaches the conducting material comprises a refractory metal.

Regarding claim 34, Jaskie ('215) teaches forming the field emitter tip and the second insulating layer. Since the Applicant has not disclosed any criticality, the order is an obvious choice in design.

Regarding claim 31, Tjaden ('223) teaches the forming a first insulating layer and the conducting gate layer comprises: forming a first insulating material; forming a conducting gate material; patterning the first insulating material and the conducting gate material at the same time.

The reason for combining is the same as for claim 20 above.

Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jaskie et al. (US 5,606,215), of record, in view of Doan et al. (US 5,259,799).

Regarding claim 21, Jaskie ('215) teaches all of the claimed limitations except for the insulating material being grown on the substrate.

Further regarding claim 21, Doan ('799) teaches that the insulating layer is grown through oxidation for the purpose of saving time and cost during the manufacturing process.

Hence it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the growing method of Doan on the display of Jaskie for the purpose of saving time and cost during the manufacturing process.

Claims 33 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jaskie et al. (US 5,606,215), of record, in view of Den et al. (US 6,628,053).

Regarding claim 33, Jaskie ('215) teaches all of the claimed limitations except for the use of nanotubes.

Further regarding claim 33, Den ('053) teaches the use of nanotubes for the purpose of improving the electron flow and thus the brightness of the display.

Hence it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the nanotube of Den in place of the field-emitting tip of Jaskie for the purpose of improving the electron flow and thus the brightness of the display.

Regarding claim 35, Den ('053) teaches using an anodic oxide to form the insulating layer.

The reason for combining is the same as for claim 33 above.

Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jaskie et al. (US 5,606,215), of record.

Regarding claim 36, Jaskie ('215) teaches all of the claimed limitations except for the second insulating layer being formed on the side but not the top surface of the gate layer.

However, there appears to be no criticality in the specification for this limitation and since Jaskie teaches the gate layer having an insulating layer for the claimed purpose, it appears that placing the insulating layer only on the side of the gate and not the top is an obvious choice in design.

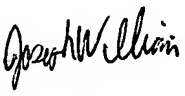
Hence it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the teaching of Jaskie for make a field emission display with an arc suppressor. Placing the insulating layer only on the side of the gate and not the top is an obvious choice in design.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph L. Williams whose telephone number is (571) 272-2465. The examiner can normally be reached on M-F (6:30 AM-3:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimeshkumar D. Patel can be reached on (571) 272-2457. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Joseph Williams
Primary Examiner
Art Unit 2879